

Notice of Allowability

Application No.

10/802,317

Examiner

Jason M. Perilla

Applicant(s)

LAI, JYH-TING

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the amendment filed August 23, 2007.
2. ☒ The allowed claim(s) is/are 1-10.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413),
Paper No./Mail Date 20071018.
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. Claims 1-10 are pending in the instant application.
2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR § 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Dan McClure on October 12, 2007.

The application has been amended as follows wherein the following versions of claims 1, 3, 5, 6, and 10 replace all prior versions in their entirety:

1. A pipelined adaptive decision feedback equalizer for equalizing a signal received from a channel, comprising:

a pre-processing unit (PP) comprising a plurality of PP coefficients for filtering the signal, and generating a PP output signal;

a feedforward filter (FFF) comprising a plurality of FFF coefficients, coupled to the pre-processing unit to receive the PP output signal;

an adder coupled to the PP feedforward filter and outputting an added signal;

a slicer coupled to the output terminal of the adder, the slicer outputting a decision signal based on the added signal;

a feedback filter (FBF) comprising a plurality of FBF coefficients, coupled to the slicer for receiving the decision signal, the feedback filter canceling post-cursor ISI and generating a FBF output signal;

a delay unit coupled between the feedback filter and the second input terminal of the adder, the delay unit receiving the FBF output signal and generating the a delayed FBF output signal to the adder, wherein the delay unit is a n_1 -tap delay block, n_1 is positive integer and $n_1 \geq 2$;

a first weight-update block for adapting the FBF coefficients to cancel the post-cursor ISI and selecting a plurality of mapping coefficients from the FBF coefficients; and

a mapping circuit for translating the plurality of mapping coefficients by a predetermined method to generate the PP coefficients and outputting the PP coefficients to the pre-processing unit, wherein at least one element of the ~~set of the~~ plurality of mapping coefficients is different from the a corresponding element of the ~~set of the~~ PP coefficients.

3. The pipelined adaptive decision feedback equalizer of claim 1, further comprises:

~~a feedforward filter comprising a plurality of FFF coefficients, coupled between the pre-processing unit and the first input terminal of the adder, the feedforward filter canceling pre-cursor intersymbol interference (ISI) from the PP output signal and generating a FFF output signal to the adder;~~

a second weight-update block for adapting the FFF coefficients to cancel the pre-cursor ISI.

5. The pipelined adaptive decision feedback equalizer of claim 1, wherein, in the mapping circuit, a relation between the mapping coefficient a_i and the PP coefficient b_j is

$$(1 - \sum_{i=1}^M a_i x^i)(1 + \sum_{j=1}^N b_j x^j) = 1 + \sum_{k=1}^{M+N} c_k x^k, \exists c_k = 0 \quad \text{if } 0 < k < n_1;$$

wherein M is the a number of the mapping coefficient, N is the a number of the PP coefficient and M , N , i , j and k are positive integers.

6. A decision feedback equalizer for equalizing a signal received from a channel, comprising:

a pre-processing unit (PP) comprising n_1 PP coefficients and a first delay unit, the pre-processing unit filtering the signal, and generating a PP output signal, wherein the first delay unit is a n_1 -tap delay block, n_1 is positive integer and $n_1 \geq 2$;

a feedforward filter (FFF) comprising a plurality of FFF coefficients, coupled to the pre-processing unit to receive the PP output signal, the feedforward filter canceling pre-cursor intersymbol interference (ISI) and outputting a FFF output signal;

an adder having a first input terminal, a second input terminal and an output terminal, the first input terminal coupled to the feedforward filter, the output terminal outputting an added signal;

a slicer coupled to the output terminal of the adder, the slicer outputting a decision signal based on the added signal;

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a feedback filter (FBF) comprising n_2 FBF coefficients and a third delay unit, coupled to the slicer, the feedback filter canceling post-cursor ISI and outputting a FBF output signal, wherein the third delay unit is a n_3 -tap delay block, n_2 and n_3 are positive integers and $n_2 = n_3 + n_1$;

a delay unit coupled between the feedback filter and the second input terminal of the adder, the delay unit receiving the FBF output signal and generating a delayed FBF output signal to the second input terminal of the adder, wherein the delay unit is a n_1 -tap delay block;

a first weight-update block for adapting the FBF coefficients to cancel the post-cursor ISI and selecting n_4 mapping coefficients from the FBF coefficients, wherein n_4 is the natural number and $n_4 \geq n_1$; and

a mapping circuit for translating the mapping coefficients by a predetermined method to generate the PP coefficients and outputting the PP coefficients to the pre-processing unit, wherein at least one element of the set of the mapping coefficients is different from the a corresponding element of the set of the PP coefficients.

10. The pipelined adaptive decision feedback equalizer of claim 6, wherein, in the mapping circuit, a relation between the mapping coefficient a_i and the PP coefficient b_j is

$$(1 - \sum_{i=1}^M a_i x^i)(1 + \sum_{j=1}^N b_j x^j) = 1 + \sum_{k=1}^{M+N} c_k x^k, \exists c_k = 0 \quad \text{if } 0 < k < n_1;$$

wherein M is the a number of the mapping coefficient, N is the a number of the PP coefficient and M , N , i , j and k are positive integers.

Allowable Subject Matter

3. Claims 1-10 are allowed.


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


Jason M. Perilla
October 18, 2007

jmp


CHIEH M. FAN
SUPERVISORY PATENT EXAMINER

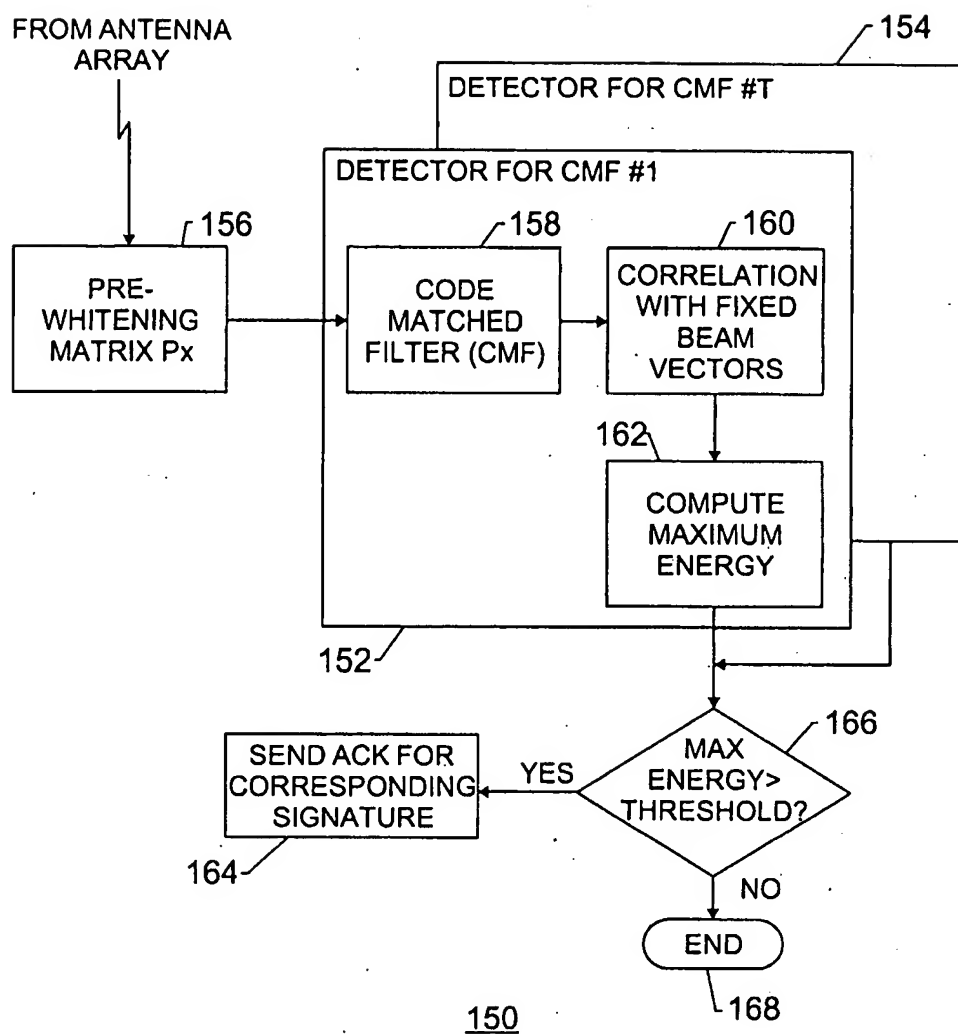


FIG. 4